1. **(Currently amended)** An in-chip monitoring apparatus, comprising:

a test pad;

a transmission gate attached to a surface of a substrate and coupled to the test pad;

a plurality of electrical components attached to **the surface** ~~a surface~~ of **the substrate** ~~a substrate~~, wherein the plurality of electrical components includes a plurality of test components coupled to the transmission gate; and

a logic block operatively coupled to the transmission gate, the logic block **operable** to receive a code word uniquely associated with one of the plurality of test components~~, the logic block~~ **and** to control operation of the transmission gate in order to route**, based on the code word,** a signal outputted by the one of the plurality of test components to the test pad.

2. **(Original)** An apparatus as in Claim 1, wherein the transmission gate is a multiplexer.

3. **(Original)** An apparatus as in Claim 1, wherein the code word has a variable bit length.

4. **(Original)** An apparatus as in Claim 1, wherein the code word has a bit length of four bits.

5. **(Currently amended)** An apparatus as in Claim 1, further comprising:

a code word generator to automatically generate **a plurality of code words** ~~the code word~~ and to automatically transmit **each of the plurality of code words separately** ~~the code word~~ to the logic block.

6. **(Original)** An apparatus as in Claim 5, wherein the code word generator is a computer.

7. **(Original)** An apparatus as in Claim 5, wherein the code word generator is incorporated as one of the plurality of electrical components on the substrate.

8. **(Original)** An apparatus as in Claim 1, further comprising:

a computer coupled to the test pad the computer to process and analyze signals received from the one of the plurality of test components.

9. **(Currently amended)** An apparatus as in Claim 1, wherein the test pad is attached to the surface of the substrate ~~**on which are placed**~~ **and wherein** a plurality of electrical components **are attached to the surface of the substrate**.

10. **(Original)** An apparatus as in Claim 1, wherein the test pad is operatively coupled to a connector attached to the substrate and wherein the test pad is operatively coupled to the transmission gate.

11. **(Currently amended)** A method, comprising:

generating a first code word of variable bit ~~**length**~~ **length;**

uniquely associating the first code word with one of a plurality of test components that are included within a plurality of electrical components; and

transmitting the first code word to a first transmission gate that is operatively coupled with the at least one of the plurality of the test components.

12. **(Currently amended)** A method as in **Claim 11** ~~**claim 8**~~, wherein the step of uniquely associating the first code word with one of the plurality of the test components further comprises:

addressing the code word to the one of the plurality of test components.

13. **(Currently amended)** A method of on-chip monitoring, the method comprising:

attaching a plurality of electrical components to a surface of a substrate;

connecting the plurality of electrical components with each other, the plurality of electrical components including a lesser plurality of test components;

attaching a plurality of test pads to the surface of the substrate, wherein the plurality of test pads is less than the plurality of test components;

coupling two or more of the plurality of test components to a transmission gate attached to the surface of the substrate; ~~and~~

coupling the transmission gate to one of the test pads**; and**

transmitting to the transmission gate a code word, the code word being uniquely associated with one of the two or more of the plurality of test components coupled to the transmission gate.

14. **(Currently amended)** A method as in ~~claim 13~~ **Claim 13**, comprising:

testing ~~the circuit~~ **one of the plurality of test components**.

15. **(Currently amended)** A method as in Claim 14, wherein the step of testing **one of the plurality of test components** ~~the circuit~~ further comprises:

~~transmitting to the transmission gate a code word, the code word being uniquely associated with one of the two or more of the plurality of test components coupled to transmission gate~~;

receiving a signal from the one of the two or more of the plurality of test components; and

analyzing the signals.

16. **(Currently amended)** A method of in-chip monitoring, comprising:

attaching a plurality of test pads to the surface of a substrate, wherein plurality of test pads is less than a plurality of test components included within a plurality of electrical components attached to the surface of the substrate;

coupling two or more of the plurality of test components to a transmission gate attached to the surface of the substrate; ~~and~~

coupling the transmission gate to a one of the test pads**; and**

transmitting to the transmission gate a code word uniquely associated with one of the two or more test components coupled to the transmission gate.

17. **(Currently amended)** A method as in Claim 16, further comprising:

testing ~~the circuit~~ **one of the plurality of test components**.

18. **(Currently amended)** A method as in Claim 16, further comprising:

monitoring ~~the circuit~~ **one of the plurality of test components**.

19. **(Currently amended)** A method as in Claim 17, wherein the step of testing ~~the circuit~~ **one of the plurality of test components** further comprises:

~~transmitting to the transmission gate a code word uniquely associated with one of the two or more of the plurality of test components coupled to the transmission gate;~~

receiving a signal from the one of the two or more of the plurality of the test components; and

analyzing the signal.